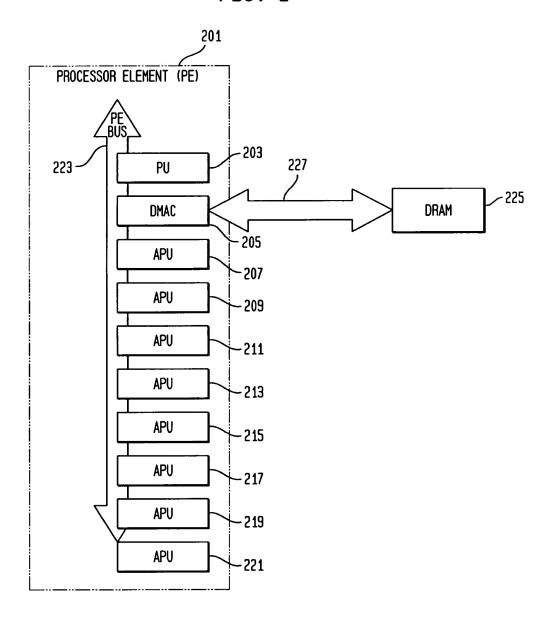




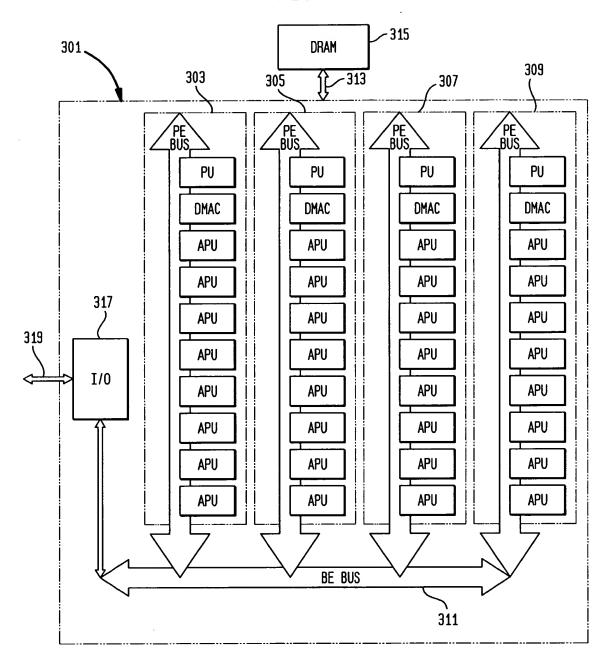
2/42 FIG. 2





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FIG. 3





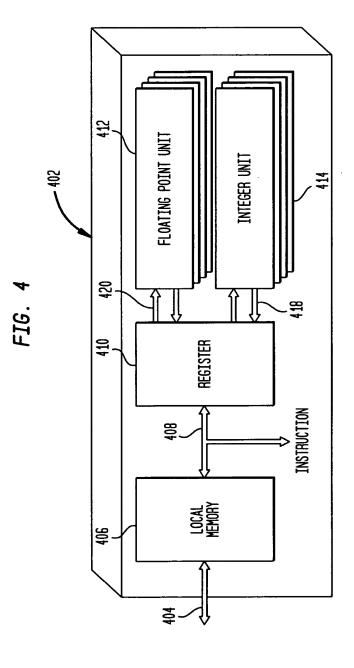
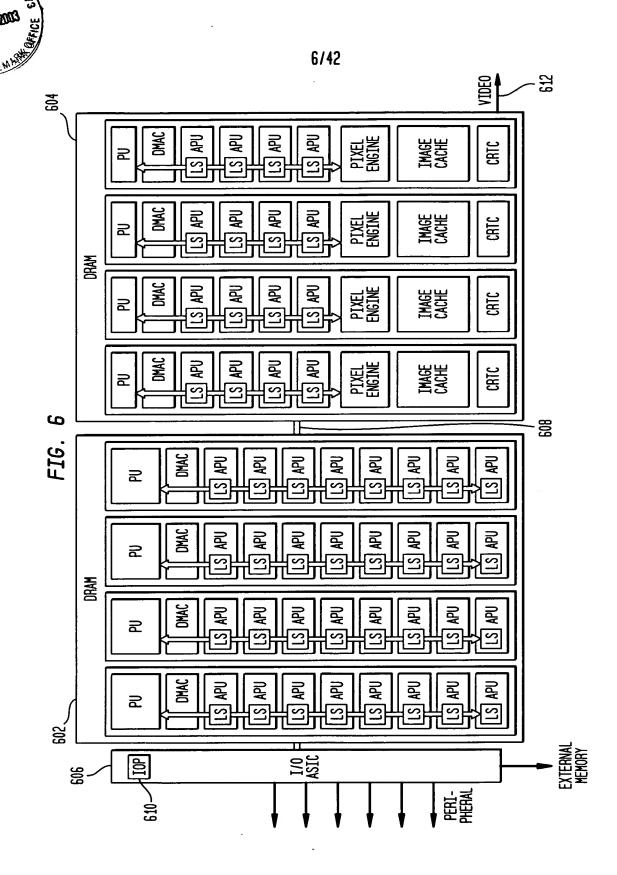


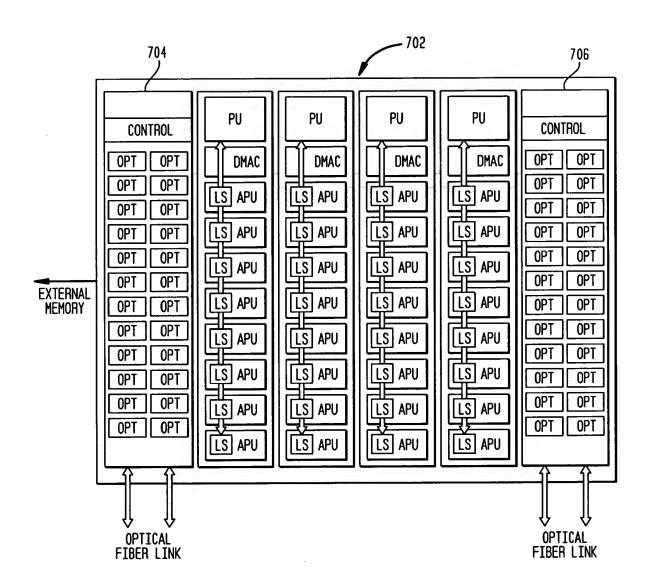


FIG. 5 -512 PU -514 < CDRAM PU CDRAM CONTROL DMAC CDRAM OPT OPT DMAC LS APU OPT OPT 516 APU APU OPT OPT -518 LS APU APU OPT OPT OPT OPT -520 APU OPT LS APU OPT -522 APU OPT OPT PIXEL ENGINE -508 OPT OPT apu OPT OPT 505~ ĹŠ APU OPT OPT 502 -IMAGE CACHE OPT OPT -510 LS APU OPT OPT 506 -504 APU CRTC

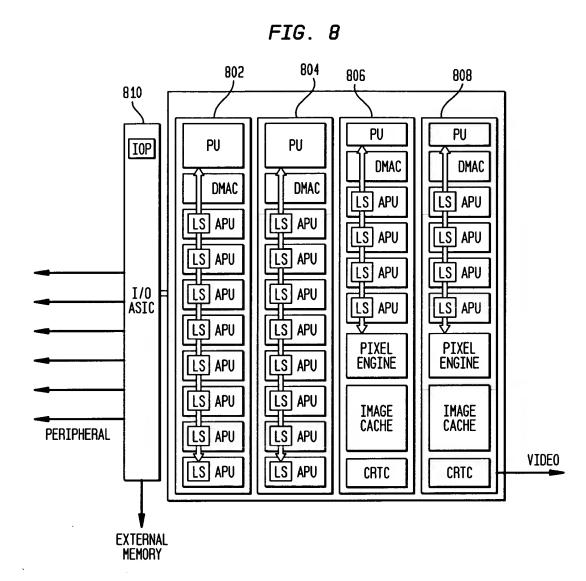




7/42 FIG. 7









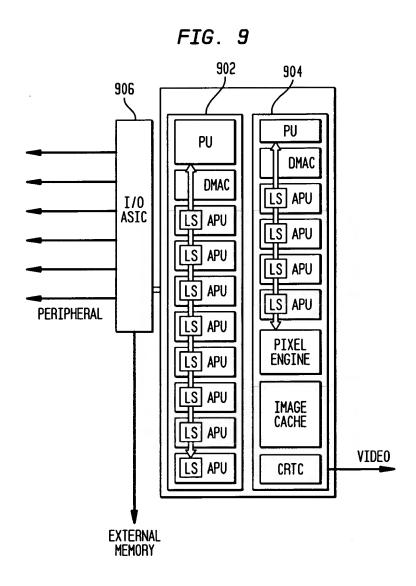
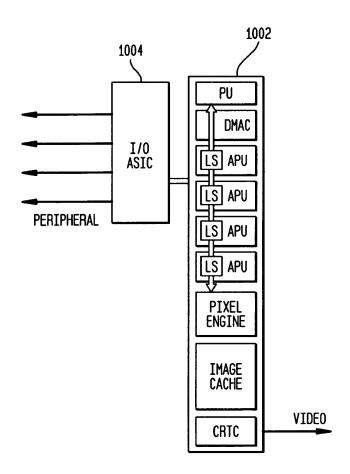
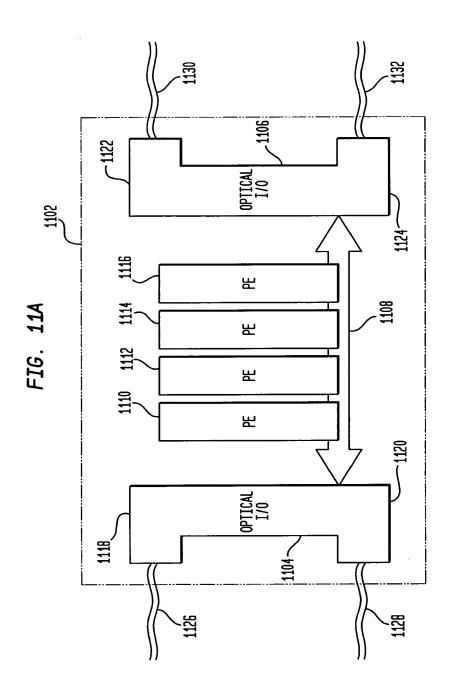




FIG. 10









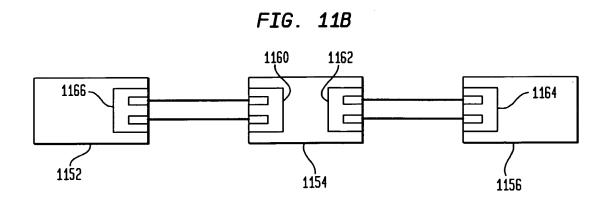
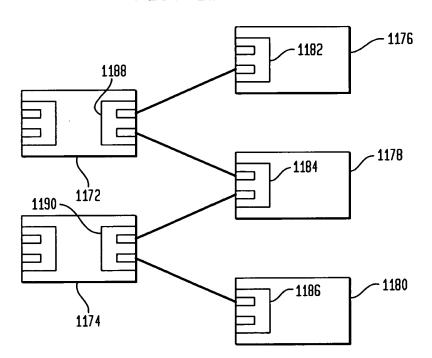
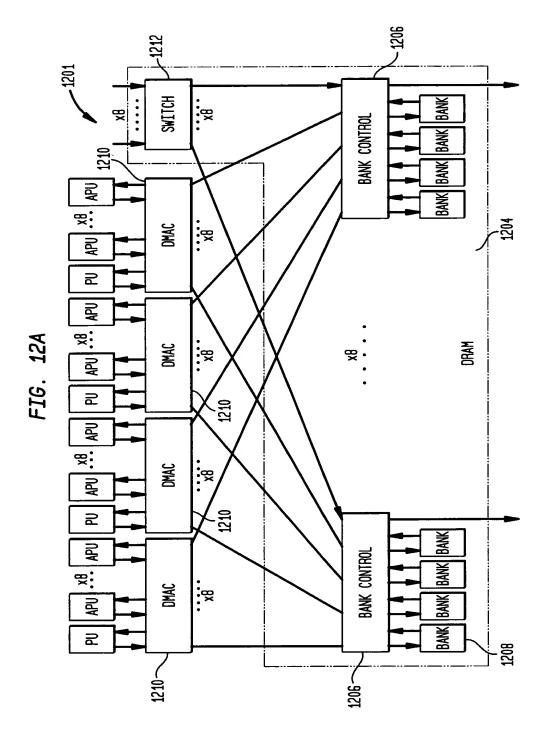


FIG. 11C









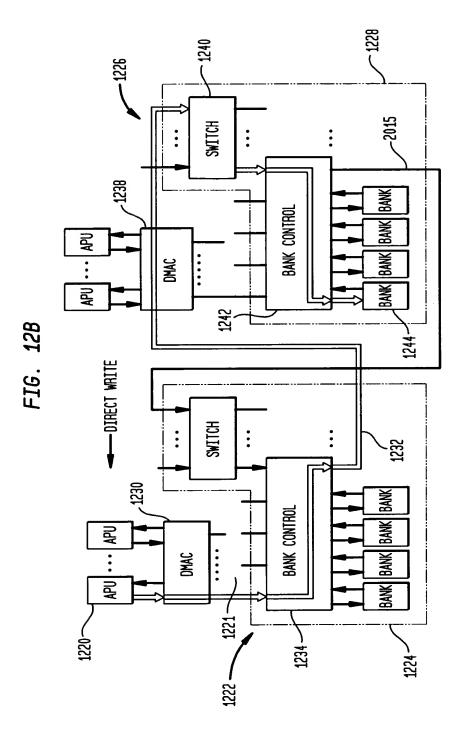
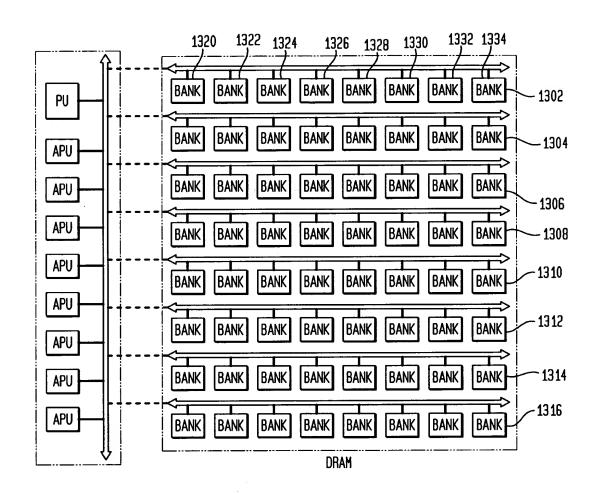




FIG. 13





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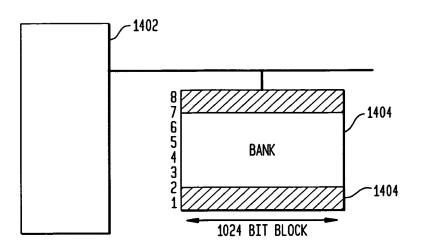
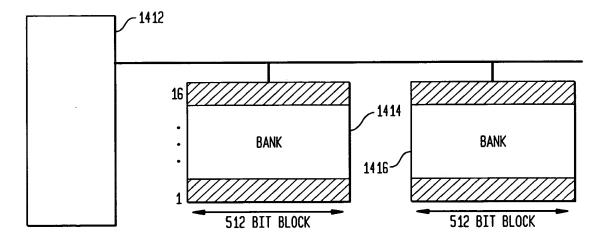
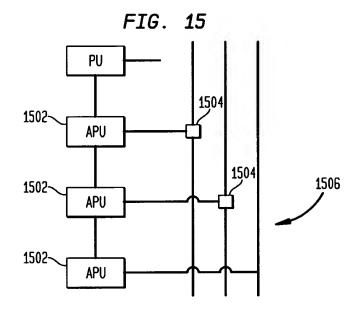
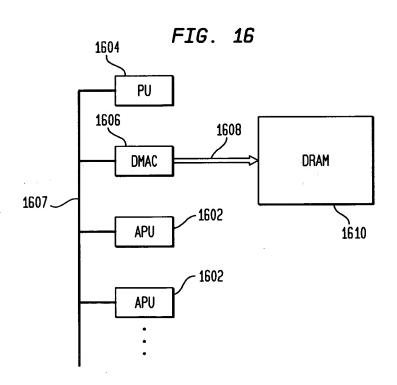


FIG. 14B











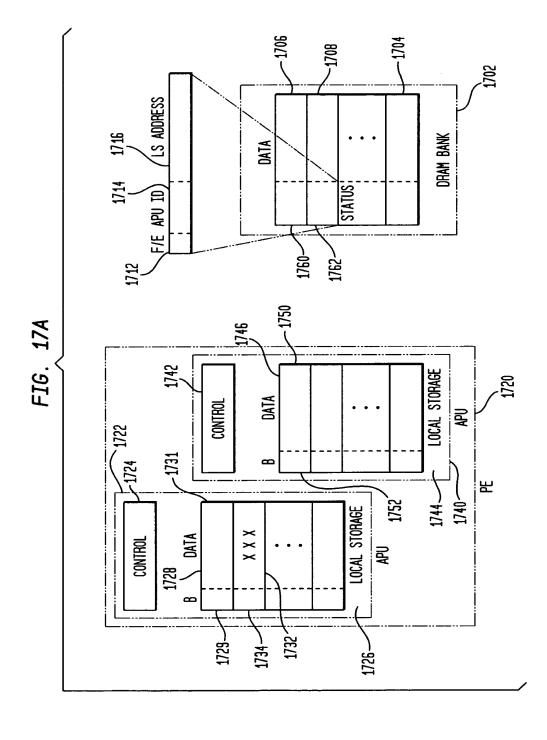
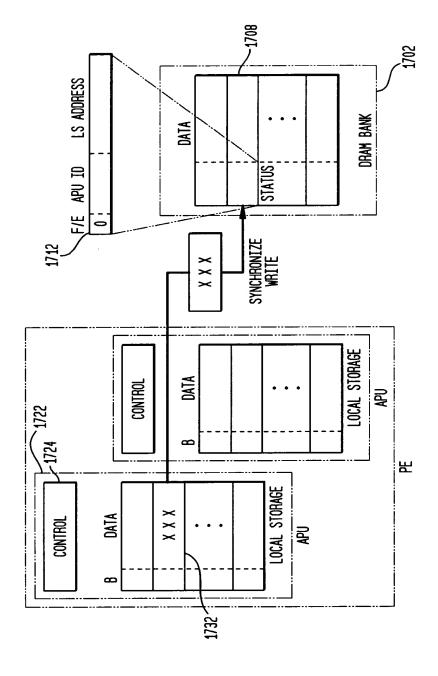
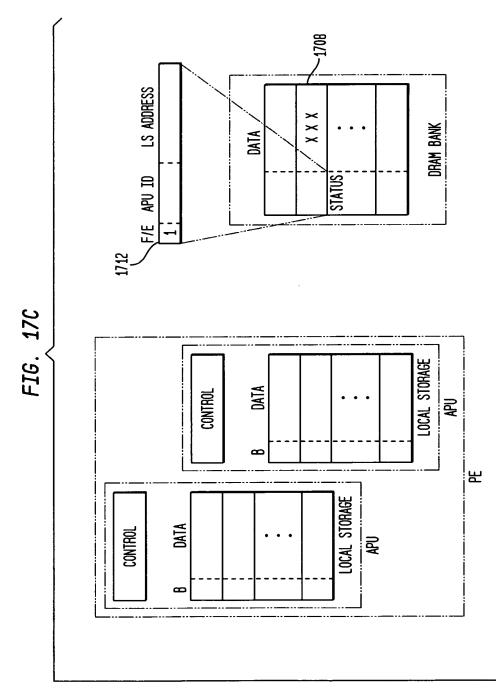




FIG. 17B









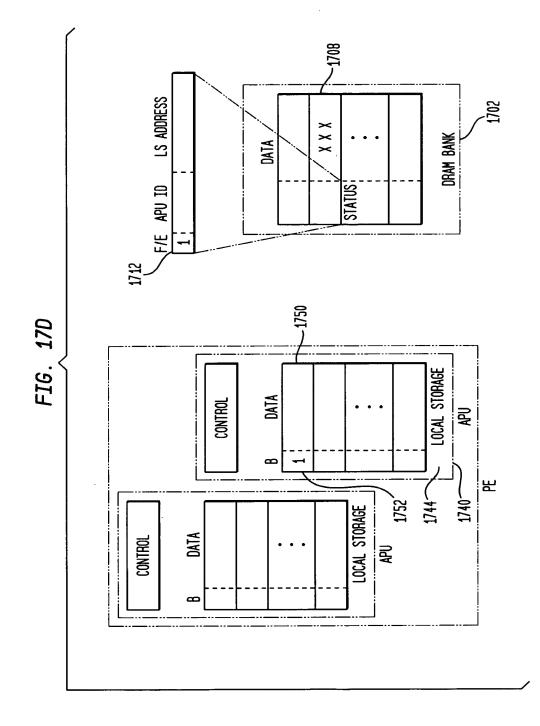
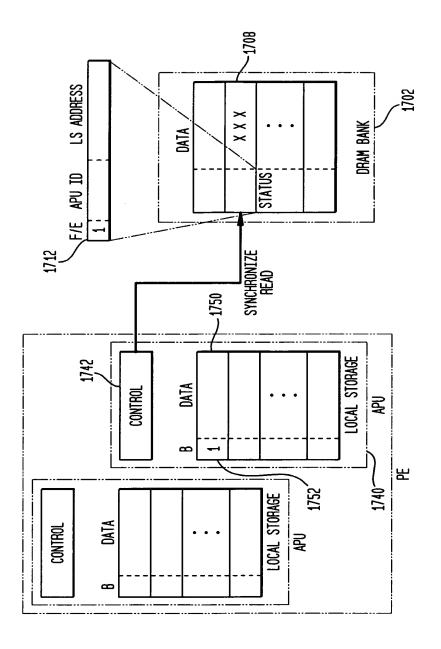




FIG. 17E





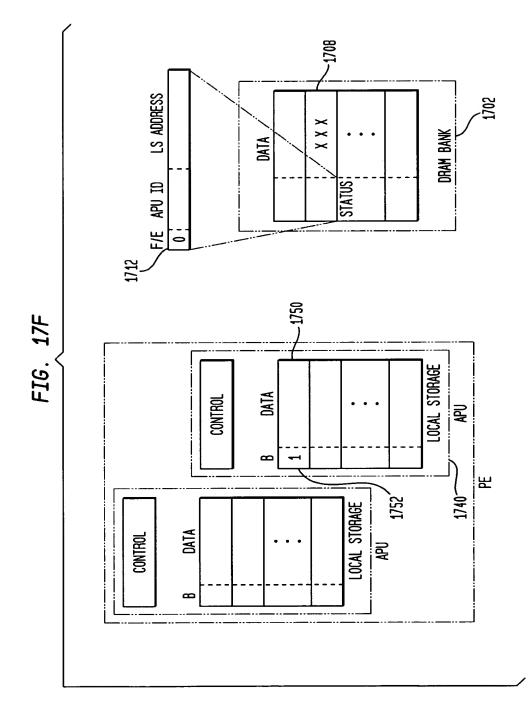
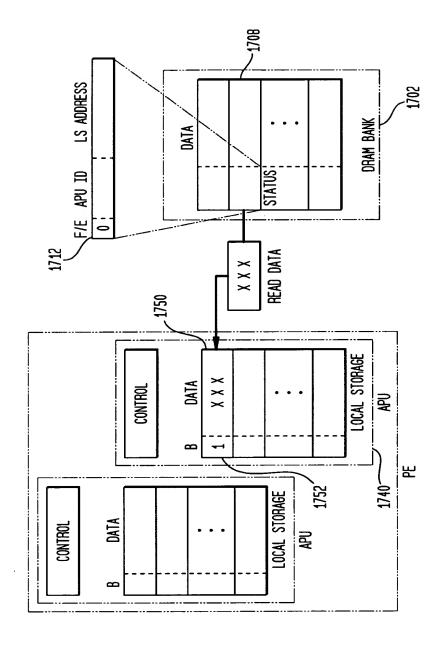
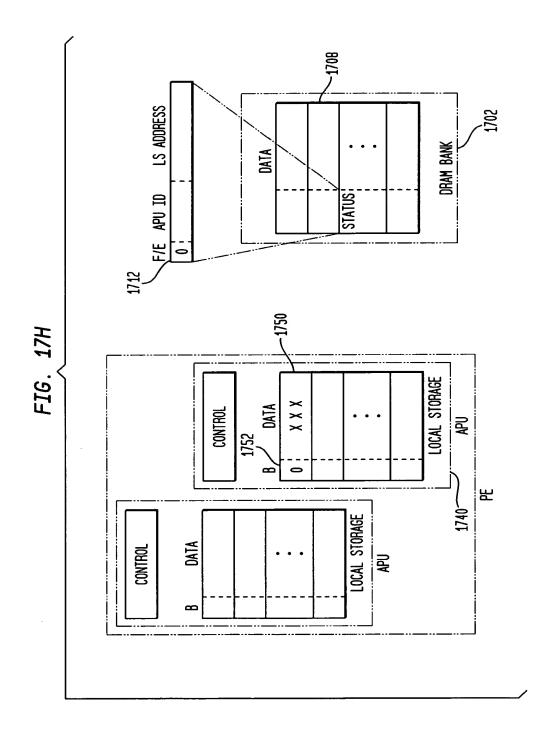




FIG. 176









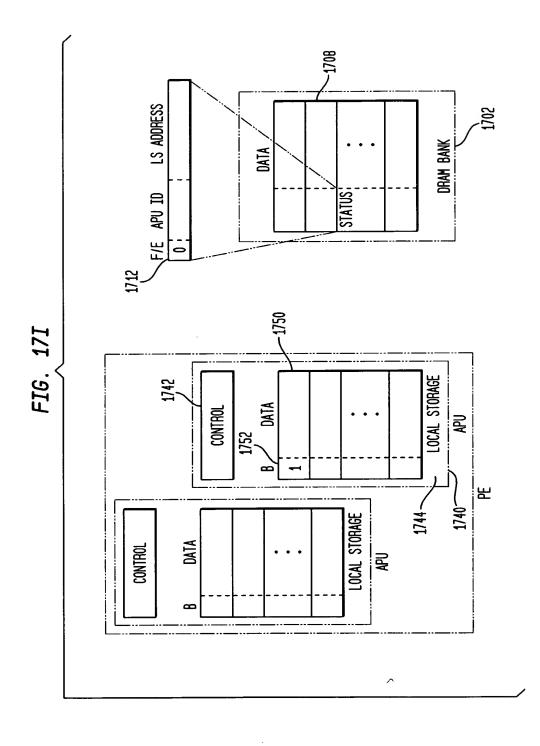
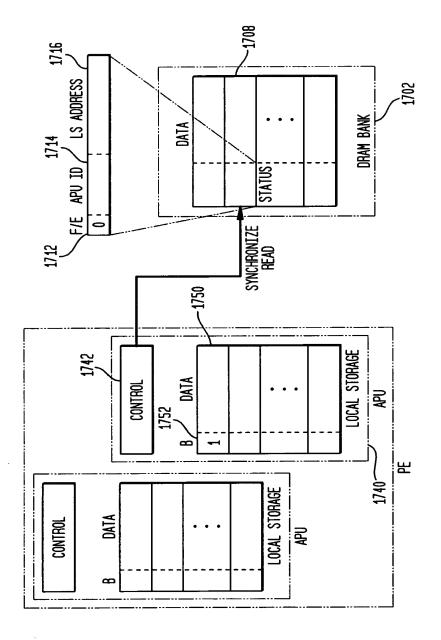




FIG. 17J





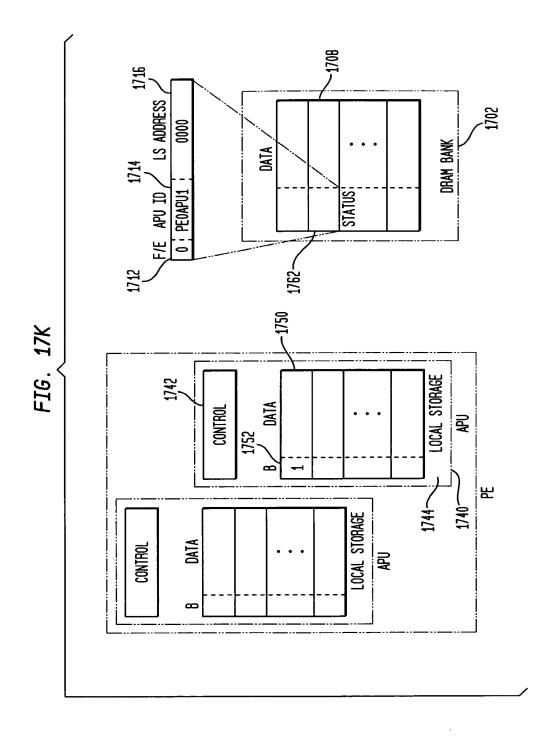
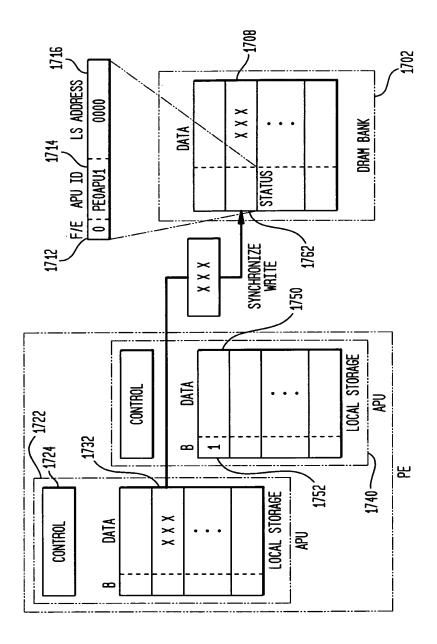




FIG. 17L





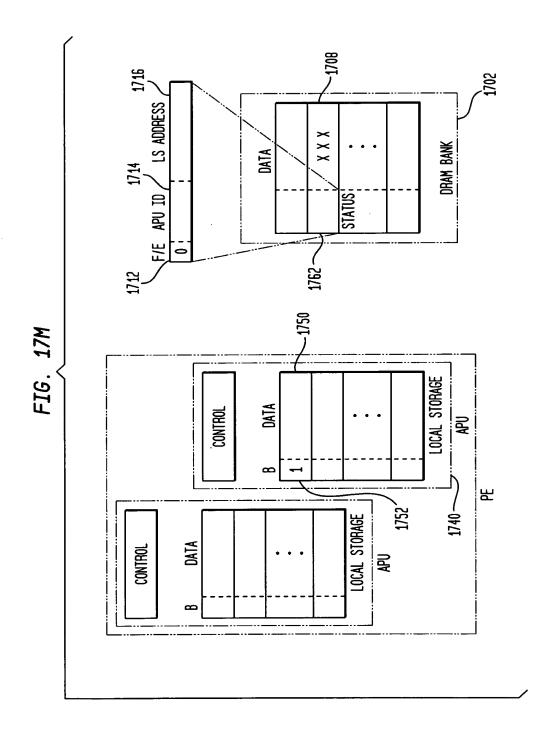
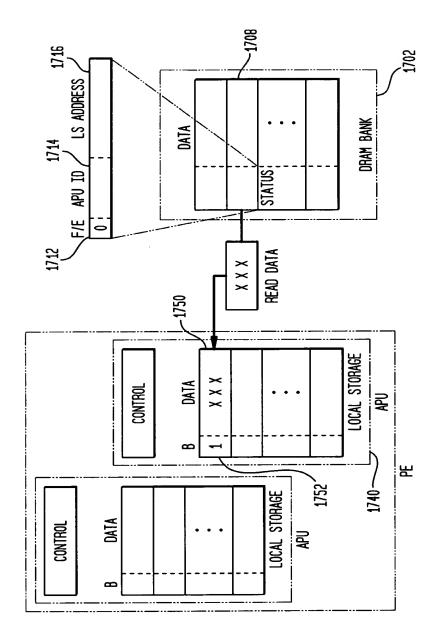




FIG. 17N





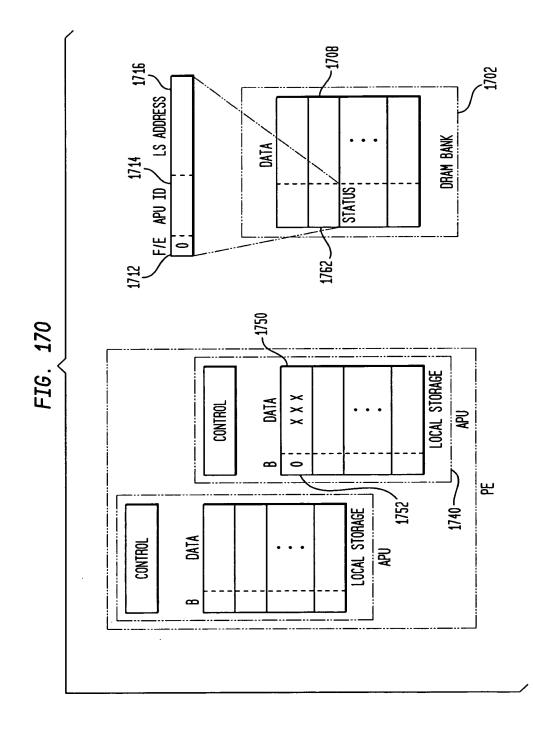




FIG. 18

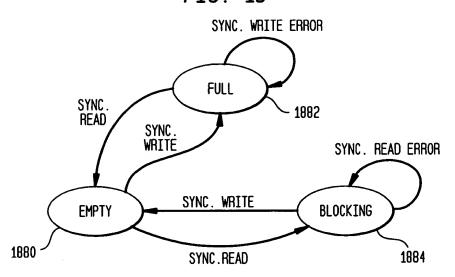


FIG. 19 1902 1908 1906 1904 ID 0 APU KEY KEY MASK 1 APU KEY KEY MASK 2 APU KEY KEY MASK APU KEY KEY MASK



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FIG. 20

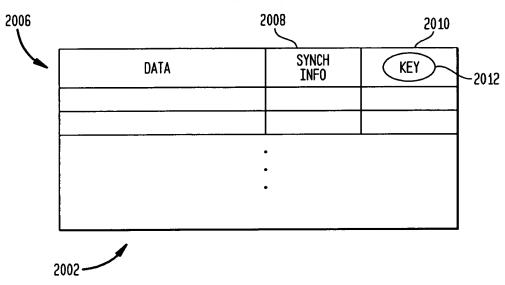


FIG. 21

	2,106		2108	2110	211
ID					
0	BASE	SIZE	ACCESS KEY	ACCESS	KEY MASK
1	BASE	SIZE	ACCESS KEY	ACCESS	KEY MASK
2	BASE	SIZE	ACCESS KEY	ACCESS	KEY MASK
		•		-	
		•			
		•			
63	BASE	SIZE	ACCESS KEY	ACCESS	KEY MASK
7					

2102



FIG. 22

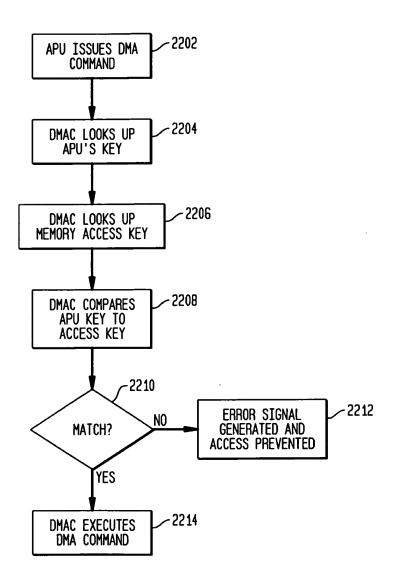
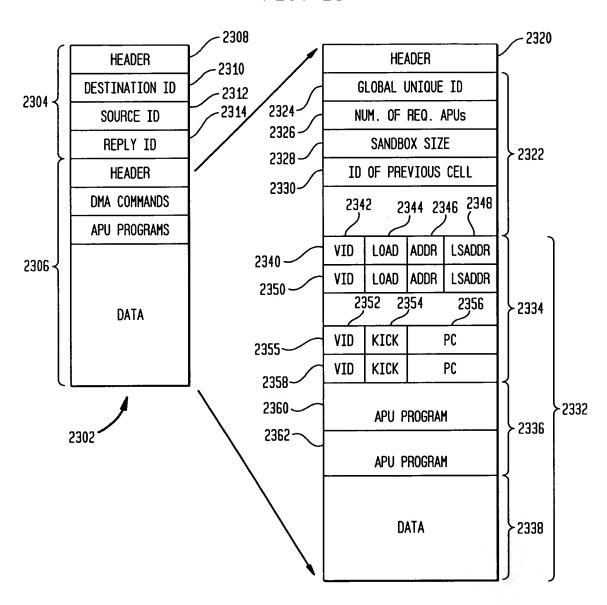
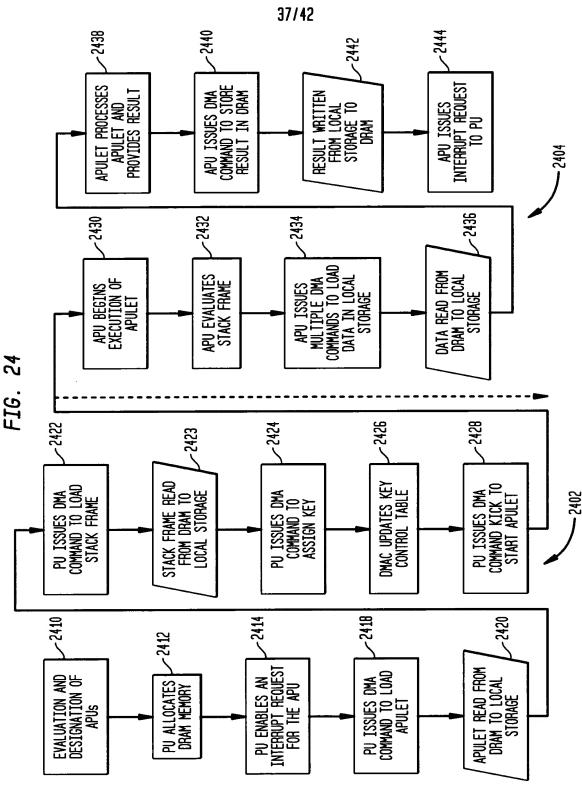


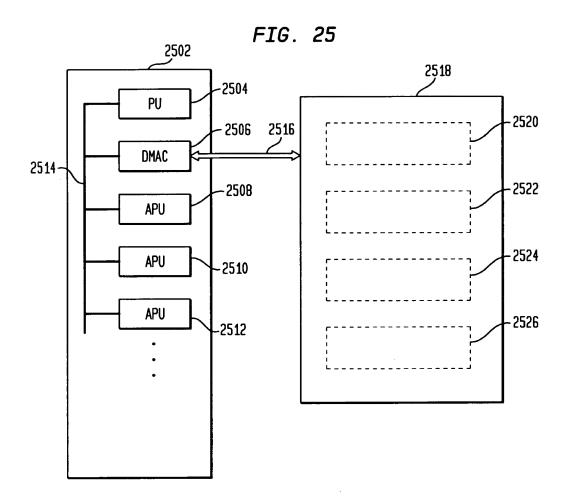


FIG. 23

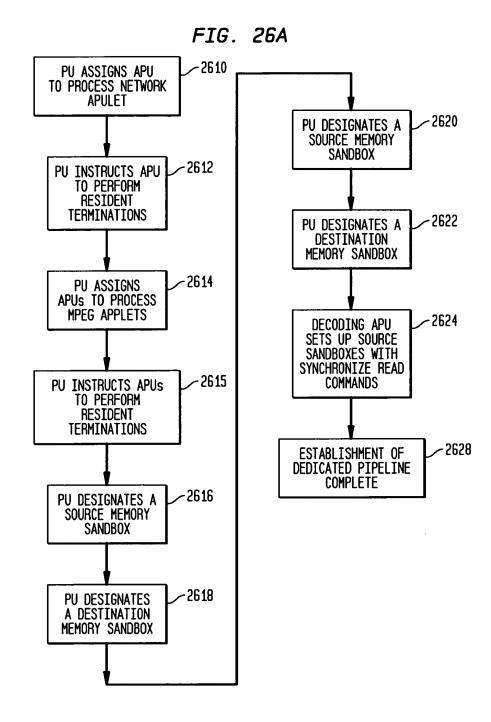














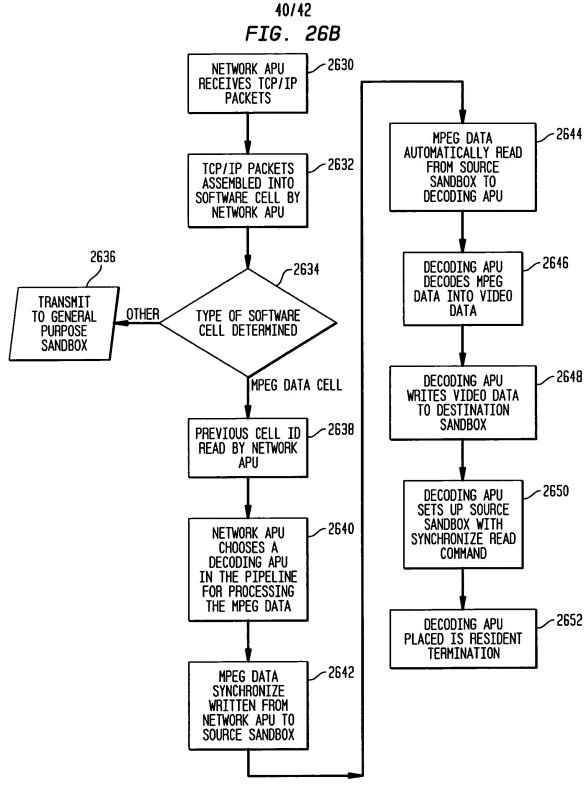
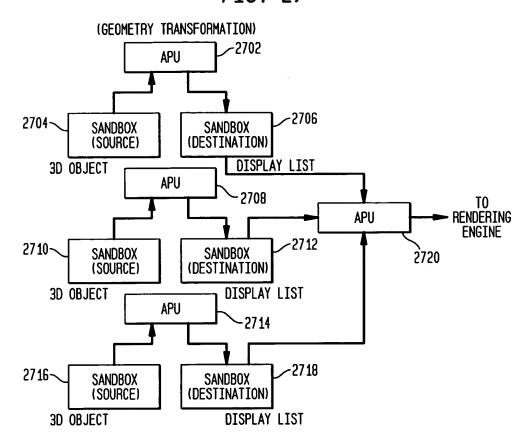




FIG. 27





 $\mathfrak{k}_{J_{s}}$

FIG. 28

